IDEC Chip Design Contest

16Gbps High Speed Interface Module with SERDES & CTLE

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Presentation Video

Abstract

Keywords – SERDES, CTLE, CDN, SDB

This study presents a high-speed SerDes circuit that achieves 16 Gbps operation within a 65 nm CMOS process, while comparable designs typically rely on more advanced nodes. In the TX mode, a 32-bit parallel signal at 500 MHz is serialized to a 1-bit 16 GHz stream using a two-stage 4-to-1 serializer and a final 2-to-1 stage. The serialized data is driven by a TSPC-based sampling flip-flop and output through an inverter chain. In the RX mode, the 16 GHz serial signal is converted to differential, equalized with a Continuous Time Linear Equalizer (CTLE), and deserialized to 32-bit parallel data.

A key strength of this work is that it delivers high-speed operation and efficient area and power usage in an older 65 nm node, compared to others relying on more advanced processes. By optimizing the architecture and using a TSPC-based clocking scheme, the design ensures reliable timing alignment and robustness. This cost-effective SerDes can be readily integrated in mass production and adapted for higher data rates.

Introduction

A. Transmitter with Serializer & Output Driver

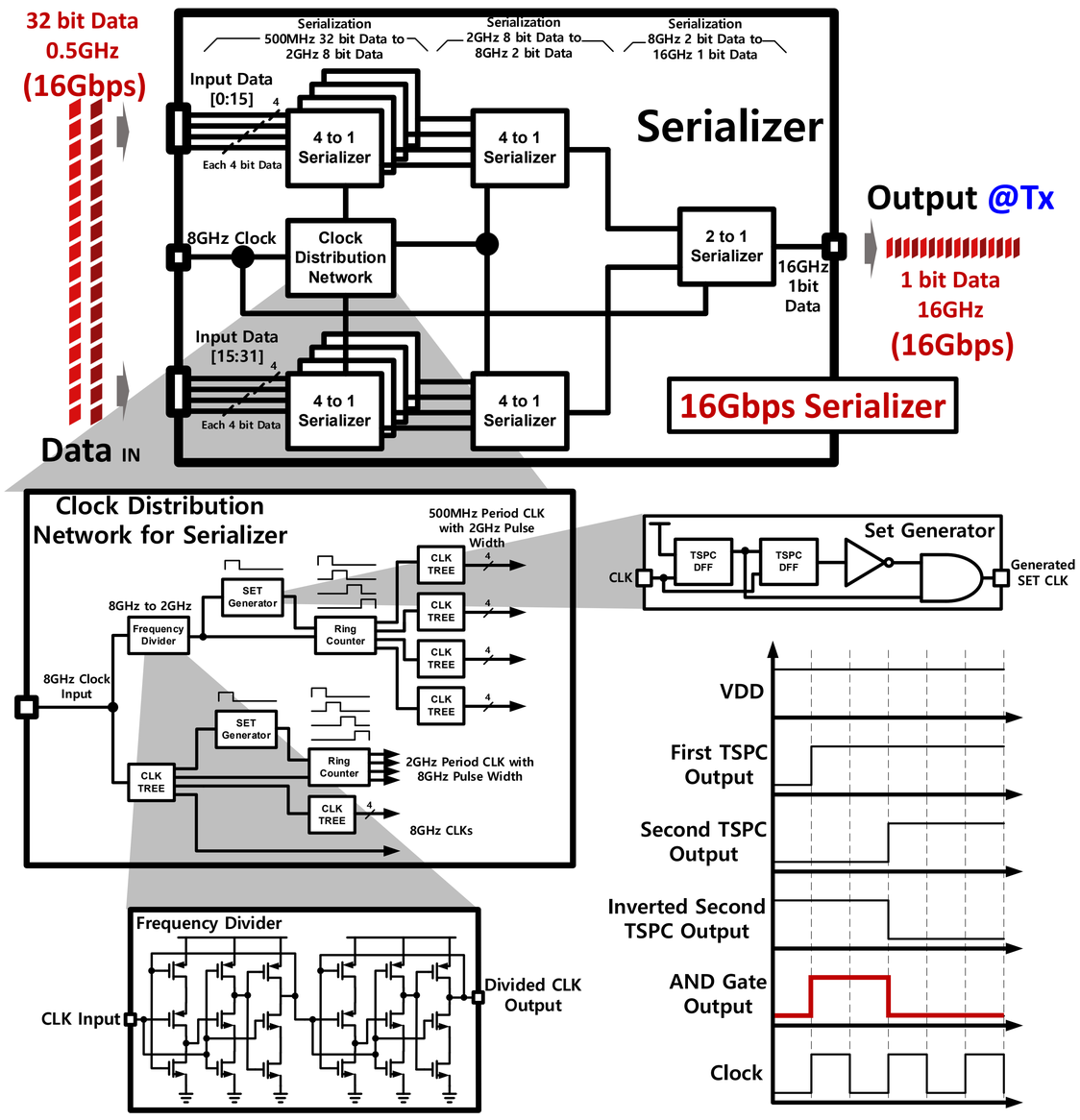

Fig 1. Serializer & CDN for Serializer Schematic & Frequency Divider & Set Generator in CDN with Set Generator Timing Diagram

This design integrates a 4-to-1 and 2-to-1 Serializer with a TSPC DFF-based Clock Distribution Network (CDN) and a recursive configuration of Transmission Gates to achieve robust data serialization in a simplified and area-efficient 65 nm CMOS implementation. A Frequency Divider and Set Generator (in Fig. 1) provide the necessary clocks, and the serialized data is driven by an Output Driver with clock doubling for high-speed output. The Receiver features a Continuous Time Linear Equalizer (CTLE) and a Single-to-Differential Buffer (SDB) with CS+CG structure, followed by a Differential CS Amplifier to attenuate noise and boost the Nyquist frequency gain by about 11 dB at 8 GHz for 16 Gbps data rates. Finally, a DET-based 1-to-2 Deserializer recovers the 32-bit parallel data, using clocks generated by the CDN.

Acknowledgement The chip fabrication and EDA tool were supported by the IC Design Education Center(IDEC), Korea.

B. Receiver with SDB w/ CTLE & Deserializer

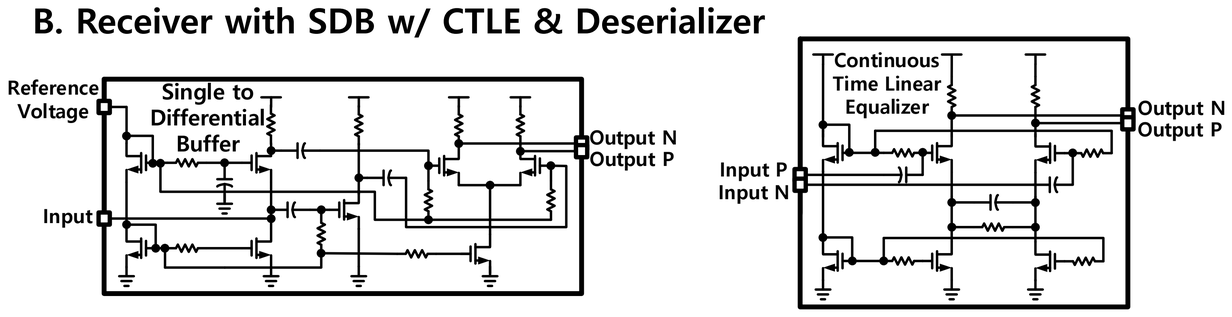

Fig 2. Single to Differential Buffer & Continuous Time Linear Equalizer

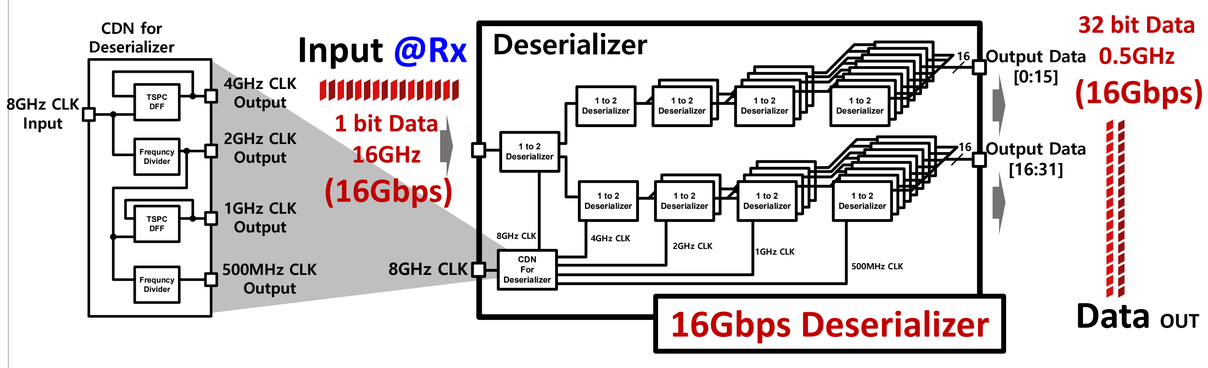

Fig 3. Deserializer & CDN for Deserializer Schematic

Results

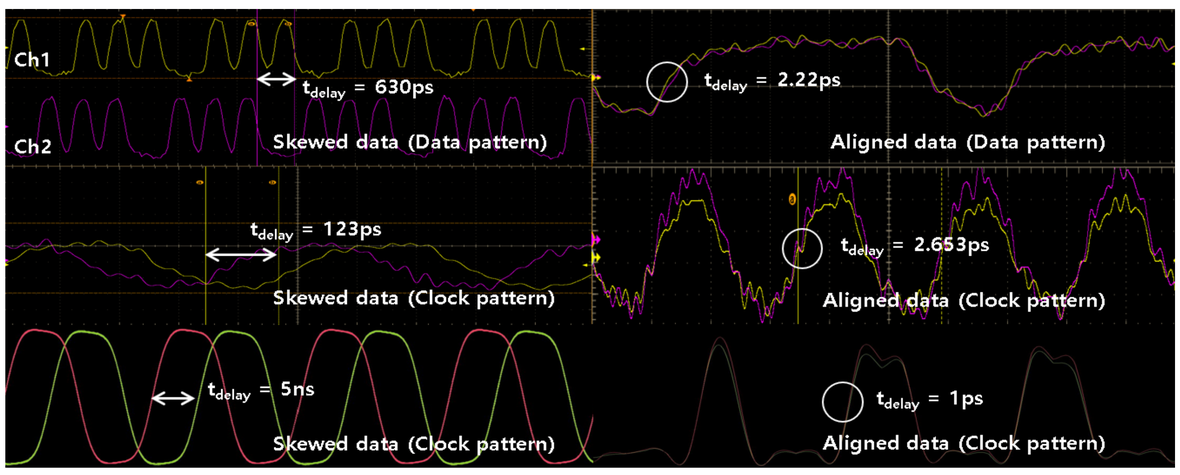

Fig 5. Clock Skewing Test Measurement Result

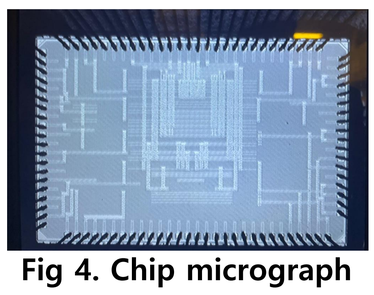

Fig 4. Chip micrograph

High FOM 1,093 is achieved

$$\text{FOM} = \frac{\text{Data Rate}}{\frac{\text{Chip Size}}{(\text{Process Channel Length})^2} \times \frac{\text{Power Consumption}}{\text{Process Channel Length}}}$$

	This Work	2010' JSSC [1]	2014' JSSC [2]	2020' JSSC [3]
Data Rate	16Gbps	Dual Lane 40Gbps	1.25G - 28.5Gbps	112Gbps
Modulation	NRZ	DQPSK	NRZ	PAM4
Chip Size	2 X 3 mm²	4 X 4 mm²	1.8 X 1.85 mm²	0.75 X 0.375 mm²
Power consumption	670mW	3W	560mW at 28Gbps	448mW
Process	65nm CMOS	65nm CMOS	28nm CMOS	10nm FinFET
FOM	**1,093**	**229**	**335**	**889**

Table 1. SERDES Specification Comparison

[1] J. Jang, H. Lim and T. W. Kim, "A CMOS Complementary Common Gate Capacitive Cross-Coupled Frequency Doubler," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 9, pp. 3694-3698, Sept. 2022

[2] S. Vehring, Y. Ding, P. Scholz and F. Gerfers, "A 3.1-dBm E-Band Truly Balanced Frequency Quadrupler in 22-nm FDSOI CMOS," in IEEE Microwave and Wireless Components Letters, vol. 30, no. 12, pp. 1165-1168, Dec. 2020

[3] Y. Ye, B. Yu, A. Tang, B. Drouin and Q. J. Gu, "A High Efficiency E-Band CMOS Frequency Doubler With a Compensated Transformer-Based Balun for Matching Enhancement," in IEEE Microwave and Wireless Components Letters, vol. 26, no. 1, pp. 40-42, Jan. 2016

Conclusion

As mentioned in previous results, this design achieves significant cost advantages in terms of chip area and power consumption compared to similar processes. It also demonstrates a certain level of efficiency when compared to more advanced processes. Therefore, this design can be robustly applied to any SERDES system utilizing a 65nm process. Furthermore, it is designed to be directly applicable to higher data rates beyond the one proposed in this paper.